DATA SHEET

SAA7710T
Dolby* Pro Logic Surround; Dolby 3 stereo; Incredible Sound

Objective specification
Supersedes data of 1996 Jul 17
File under Integrated Circuits, IC01

1997 Aug 01

Philips Semiconductors

PHILIPS

Dolby* Pro Logic Surround; Dolby 3 stereo; Incredible Sound

SAA7710T

FEATURES

- Two stereo I²S-bus digital input channels
- Three stereo I²S-bus digital output channels
- I²C-bus mode control
- Up to 45 ms on-chip delay-line (f_s = 44.1 kHz)
- Optional clock divider for crystal oscillator
- Package: SO32L
- Operating supply voltage range: 4.5 to 5.5 V.

Functions

- 4-channel active surround, 20 Hz to 20 kHz (maximum $^{j}/_{2}f_s$)
- Adaptive matrix
- 7 kHz low-pass filters
- Adjustable delay for surround channel
- Modified Dolby B noise reduction
- Noise sequencer
- Variable output matrix
- Sub woofer
- Centre mode control: on/off, normal, phantom, wide
- Output volume control
- Automatic balance and master level control with DC-offset filter
- Hall/matrix surround sound functions
- Incredible sound functions
- 3-band parametric equalizer on main channels left, centre, right (f_s = 44.1 kHz)
- 5-band parametric equalizer on main channels left, centre, right (f_s = 32 kHz)
- Tone control (bass/treble) on all four output channels (f_s = 44.1 kHz).

GENERAL DESCRIPTION

This data sheet describes the 104 ROM-code version of the SAA7710T chip. The SAA7710T chip is a high quality audio-performance digital add-on processor for digital sound systems. It provides all the necessary features for complete Dolby Pro Logic surround sound on chip.
In addition to the Dolby Pro Logic surround function, this device also incorporates a 3-band parametric equalizer, a 5-band parametric equalizer, a tone control section and a volume control. Instead of Dolby Pro Logic surround, the Hall/matrix surround and Incredible sound functions can be used together with the equalizer or tone control.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	DC supply voltage	–0.5	+6.5	V
ΔV_{DD}	voltage difference between two V_{DDx} pins	–	550	mV
V_i	maximum input voltage	–0.5	V_{DD} + 0.5	V
I_{DD}	DC supply current	–	50	mA
I_{SS}	DC supply current	–	50	mA
T_{amb}	ambient operating temperature	–40	+85	°C
T_{stg}	storage temperature range	–65	+150	°C

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7710T/N104	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

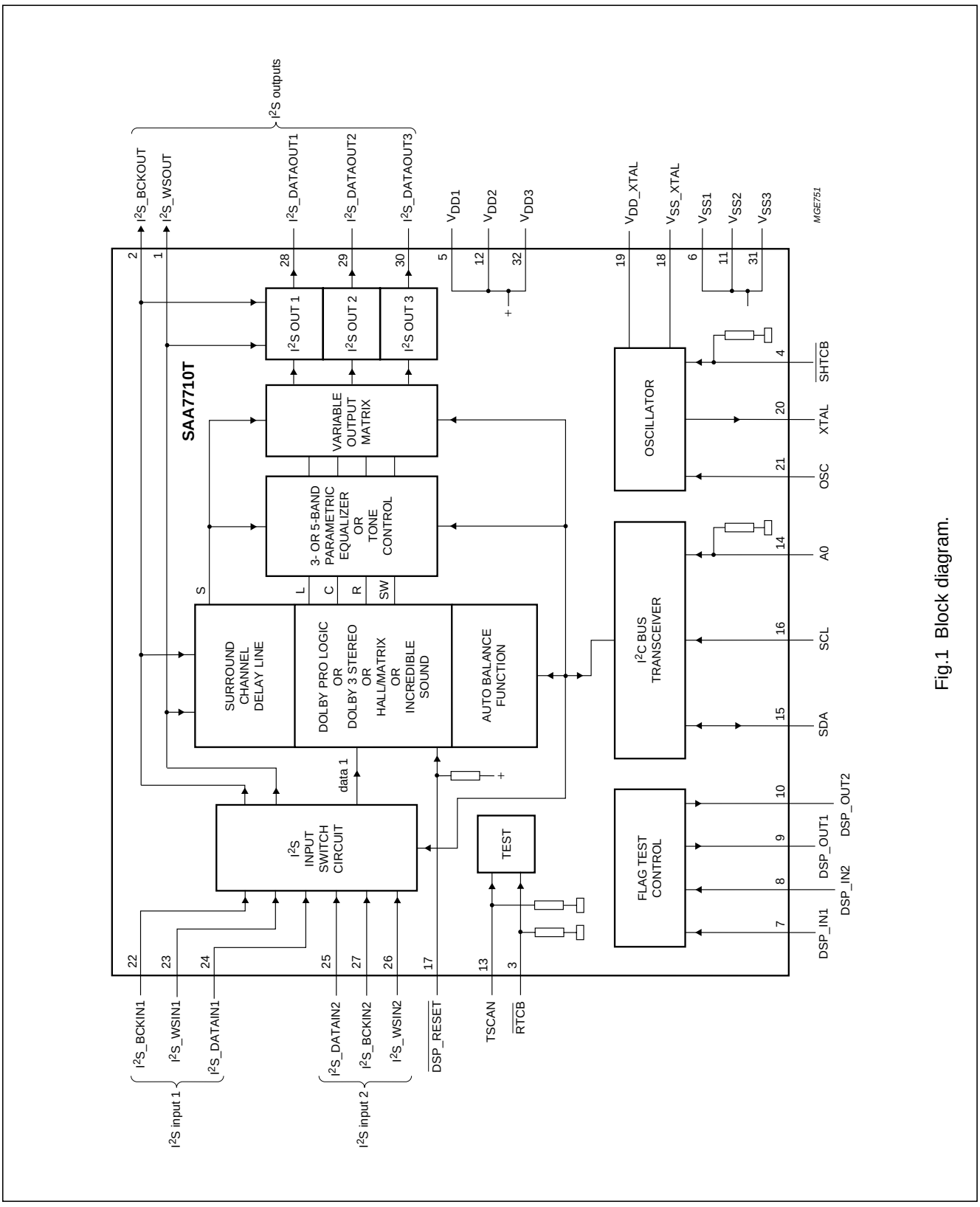


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
I^2S_WSOUT	1	I^2S-bus slave word-select output
I^2S_BCKOUT	2	I^2S-bus slave bit-clock output
$\overline{RTCB}$	3	asynchronous reset test control block input (active LOW)
$\overline{SHTCB}$	4	clock divider switch enable input (LOW = divide)
V_{DD1}	5	positive power supply
V_{SS1}	6	ground power supply
DSP_IN1	7	flag input 1
DSP_IN2	8	flag input 2
DSP_OUT1	9	flag output 1
DSP_OUT2	10	flag output 2
V_{SS2}	11	ground power supply
V_{DD2}	12	positive power supply
TSCAN	13	scan control input
A0	14	I^2C-bus slave address selection input
SDA	15	I^2C-bus serial data input/output
SCL	16	I^2C-bus serial clock input
$\overline{DSP\_RESET}$	17	chip reset input (active LOW)
V_{SS_XTAL}	18	ground power supply crystal oscillator
V_{DD_XTAL}	19	positive power supply crystal oscillator
XTAL	20	crystal oscillator output
OSC	21	crystal oscillator input
I^2S_BCKIN1	22	I^2S-bus master bit-clock input 1
I^2S_WSIN1	23	I^2S-bus master word-select input 1
I^2S_DATAIN1	24	I^2S-bus master data input 1
I^2S_DATAIN2	25	I^2S-bus master data input 2
I^2S_WSIN2	26	I^2S-bus master word-select input 2
I^2S_BCKIN2	27	I^2S-bus master bit-clock input 2
I^2S_DATAOUT1	28	I^2S-bus slave data output 1
I^2S_DATAOUT2	29	I^2S-bus slave data output 2
I^2S_DATAOUT3	30	I^2S-bus slave data output 3
V_{SS3}	31	ground power supply
V_{DD3}	32	positive power supply

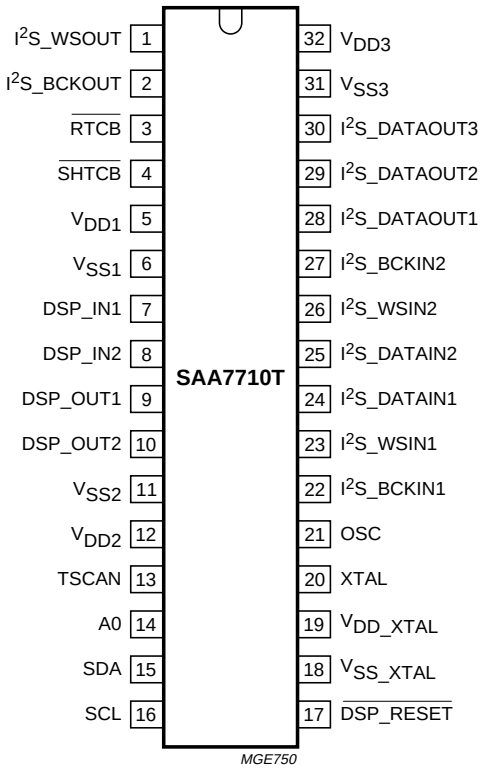


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Figure 1 shows the block diagram of the SAA7710T. The SAA7710T consists of a Dolby Pro Logic decoder together with equalizer or tone control. The Dolby Pro Logic part of the IC may be used to decode audio soundtracks (Dolby surround movies or Dolby surround video productions) from for example, a video recorder (VCR) or a CD laser disc into four channels Left, Centre, Right and Surround (L, C, R and S).
If desired, post-processing with either an equalizer or a tone control section is possible. In addition to this, a Sub Woofer (SW) channel, digital volume control and a user-programmable variable output matrix are implemented.

Hall/matrix surround sound functions are implemented for material not encoded using Dolby Surround. These features can be used as an alternative to Dolby Pro Logic and can also be combined with the equalizer or tone control sections.

Incredible sound is a Philips patented technology which substantially improves the stereo effect of a television or audio system. Using advanced signal processing, speakers that are positioned close together can imitate the sound produced by speakers that are far apart.

Functional modes

The device thus supports three main modes, Dolby Pro Logic/Dolby 3 stereo or hall/matrix surround or Incredible sound mode. All modes can be combined with equalizing (3-band or 5-band) or tone control depending on f_s and available cycle budget.

THE DOLBY PRO LOGIC MODE

In Dolby Pro Logic mode, several blocks must be initialized and controlled during operation:

- Noise generator and noise sequencer
- Centre channel mode(1) (normal, phantom, wide, off)
- Combining network coefficients
- 7 kHz low-pass filter in surround channel(1)
- Surround channel delay time(1)
- Modified Dolby B noise reduction must be on.

Possible post-processing modes for Dolby Pro Logic are:

- Volume control only
- Equalizer (3- or 5-band on L, C and R) or tone control (L, C, R and S); fixed output matrix(1); volume control
- Equalizer (5-band on L, C and R); variable output matrix(1); volume control
- Extra sub woofer(1).

THE DOLBY 3 STEREO MODE

In Dolby 3 stereo mode, several blocks must be initialized and controlled during operation:

- Noise generator and noise sequencer
- Centre channel mode(1) (normal, phantom, wide and off)
- Combining network coefficients.

THE HALL/MATRIX SURROUND MODE

In hall/matrix surround mode, the blocks listed below must be initialized and controlled during operation:

- Input balance control
- Hall or matrix surround Mode setting
- All-pass and filter transfer characteristics(1)
- 7 kHz low-pass filter in surround channel(1)
- Surround channel delay(1).

Possible post-processing modes for hall/matrix surround are as above:

- Volume control only
- Equalizer (3- or 5-band on L, C and R) or tone control (L, C, R and S); fixed output matrix(1); volume control
- Equalizer (5-band on L,C,R); variable output matrix(1); volume control
- Extra sub woofer(1).

THE INCREDIBLE SOUND MODE

In the Incredible sound mode the blocks listed below must be initialized and controlled during operation:

- Incredible sound coefficients
- Combining network coefficients.

Possible post-processing modes for incredible sound are as follows:

- Volume control only
- Equalizer (5-band on L and R) or tone control (L and R); variable output matrix(1), volume control
- Extra sub-woofer(1).

(1) The coefficient set used to initialize and control the operation of the Dolby Pro Logic mode depends upon the selected sampling frequency f_s = 32, 44.1 or 48 kHz.

ADDITIONAL INFORMATION

The possible modes of operation are discussed in more detail in the *"SAA7710T Dolby Pro Logic Programming Guide, Application Note AN95063"*. This also includes which features are available for a given system clock frequency and sample frequency and the possible input configurations.

Clock circuit and oscillator

The chip has an on board crystal clock oscillator. The block schematic of this Pierce oscillator is shown in Figs 3 and 4. The active element needed to compensate for the loss resistance of the crystal is the amplifier Gm. This amplifier is placed between the XTAL (output) pin and the OSC (sense) pin. The gain of the oscillator is internally controlled by the automatic gain control. This prevents too much power loss in the crystal. The higher harmonics are then as low as possible. The signals on the OSC and XTAL pin are differentially amplified.

The oscillator has these two modes of operation:

The crystal oscillator mode: in this mode (see Fig.3), a quartz crystal oscillator is used to generate a clock signal which is subsequently divided by 2 to ensure that the final clock signal has a 50% duty cycle.
The oscillator circuit components R_{bias} and C1, C2 depend on the crystal. In the case of an overtone oscillator, the ground harmonic is filtered out by L1 and C3. Pin $\overline{\text{SHTCB}}$ is held low so that the divided signal is selected. Only a quartz crystal should be used in this mode.

The slave oscillator mode: in this mode (see Fig.4), the oscillator circuit acts as a slave driven by a master system clock. The clock divider can be switched on or off using pin $\overline{\text{SHTCB}}$. When the divider is not used, the duty cycle of the clock will depend on the master system clock duty cycle and the rising and falling edge times. This places a tolerance of 5% on the 50% duty cycle of the master system clock (see Chapter "AC characteristics").

In order to be able to control the phase of the clock signal during testing the divider is skipped and the signal is directly fed to the circuit via the multiplexer in the TEST position.

SUPPLY OF THE CRYSTAL OSCILLATOR

The power supply connections to the oscillator are separated from the other supply lines to minimise feedback from on-chip ground bounce to the oscillator circuit. Noise on the power supply affects the AGC operation so the power supply should be decoupled. The V_{SS_XTAL} pin is used as ground supply and the V_{DD_XTAL} as positive supply.

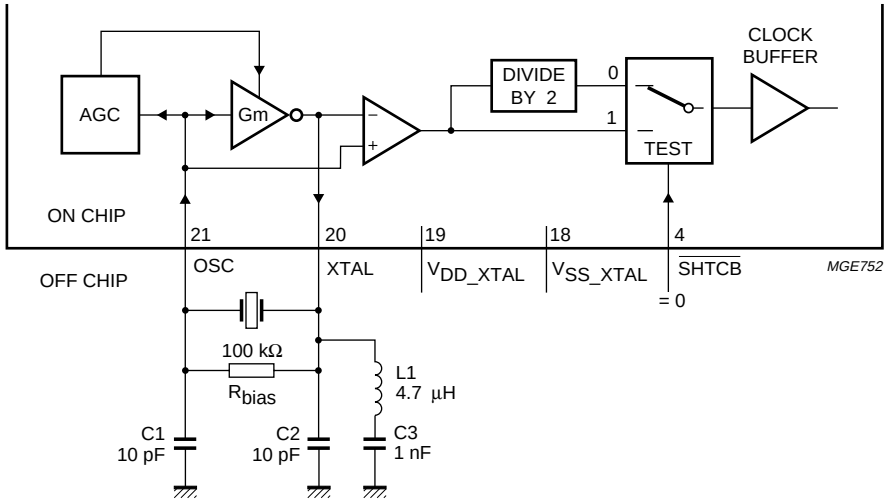


Fig.3 Block diagram crystal oscillator circuit.

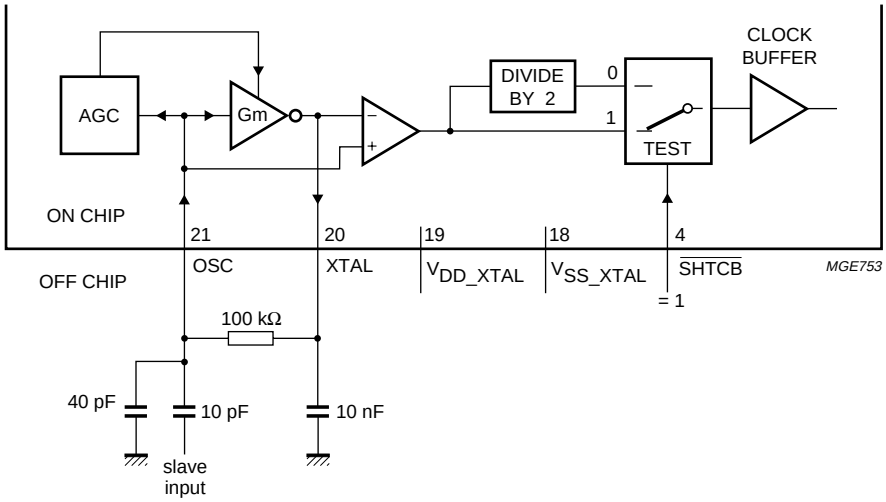


Fig.4 Block diagram slave oscillator circuit.

I²S-bus Interfaces and system clock

I²S-BUS BASICS

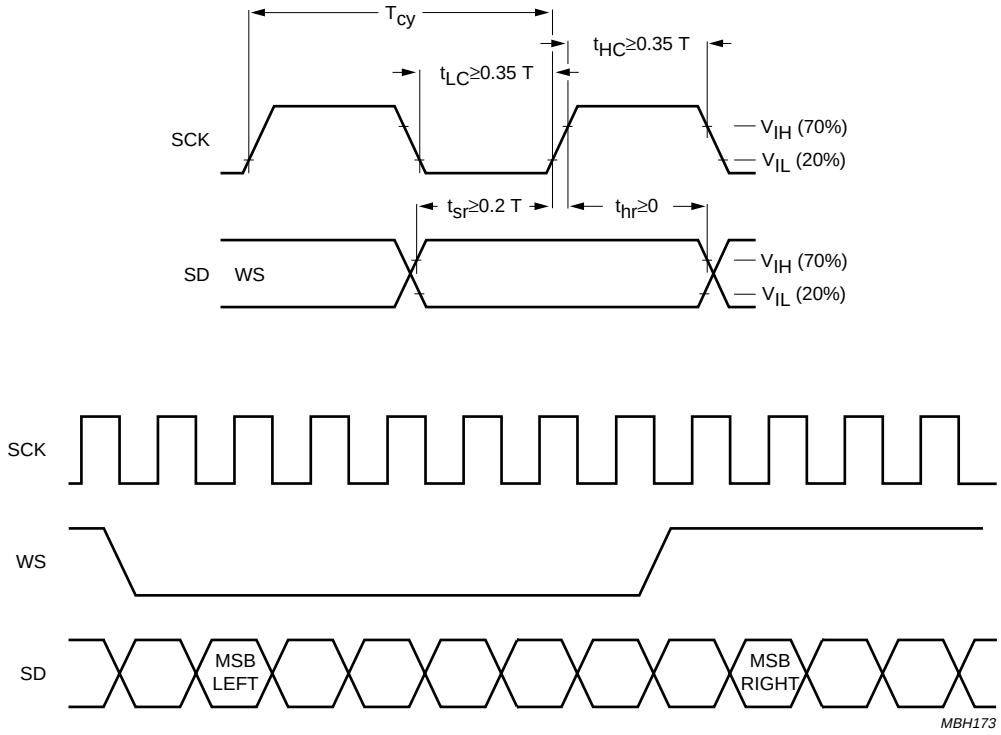


Fig.5 I²S-bus timing and format.

For communication with external digital sources and or additional external processors the I²S-bus digital interface bus is used. It is a serial 3-line bus, with one line for data, one line for clock and one line for the word select.

Figure 5 shows an excerpt of the Philips I²S-bus specification interface report regarding the general timing and format of I²S-bus. Word Select (WS) logic 0 means left channel word, logic 1 means right channel word.

The serial data is transmitted in two's complement with the MSB first. One clock period after the negative edge of the word select line the MSB of the left channel is transmitted. Data is synchronised with the negative edge of the clock and latched at the positive edge.

I²S-BUS INPUT CIRCUIT

The I²S-bus input circuits can be configured in the following way using the SEL-IN1/IN2 bit (see Table 4):

1. I²S input 1 is master
   (SEL-IN1/IN2 bit = logic 0(default))
2. I²S input 2 is master (SEL-IN1/IN2 bit = logic 1).

The incoming bit-clock frequency defines the accuracy in terms of number of bits of the incoming data samples. The input circuit is designed to accept any number of bits per channel up to a maximum of 18 bits. The accepted data format is MSB-first.

Table 1 Data Accuracy in I²S-bus Interface

INCOMING DATA WIDTH	I²S-BUS IN DATA WIDTH	I²S-BUS OUT DATA WIDTH
A < 18	A	A
B ≥18	18	18

THE I²S-BUS OUTPUT INTERFACE

The I²S-bus data output interfaces (see Fig.1) I²S OUT 1, I²S OUT 2 and I²S OUT 3 use the same I²S-bus data signals which are selected by the input switch circuit. The I²S-bus WS and BCK output signals remain in phase with the external input signals at all times. The output data is $1/f_s$ cycle delayed relative to the input data. The selected word-select and bit-clock are included as part of the output interface: I²S_WSOUT, I²S_BCKOUT. These two output signals can be 3-stated by setting the DIS_BCKWS bit (see Table 4). The 3-state output of the I²S_DATAOUT3 signal can be enabled by setting the ENA_I²S3 bit (see Table 4).

The timing diagram of the I²S-bus outputs is shown in Fig.6. The timing details can be found in Chapter “AC characteristics”.

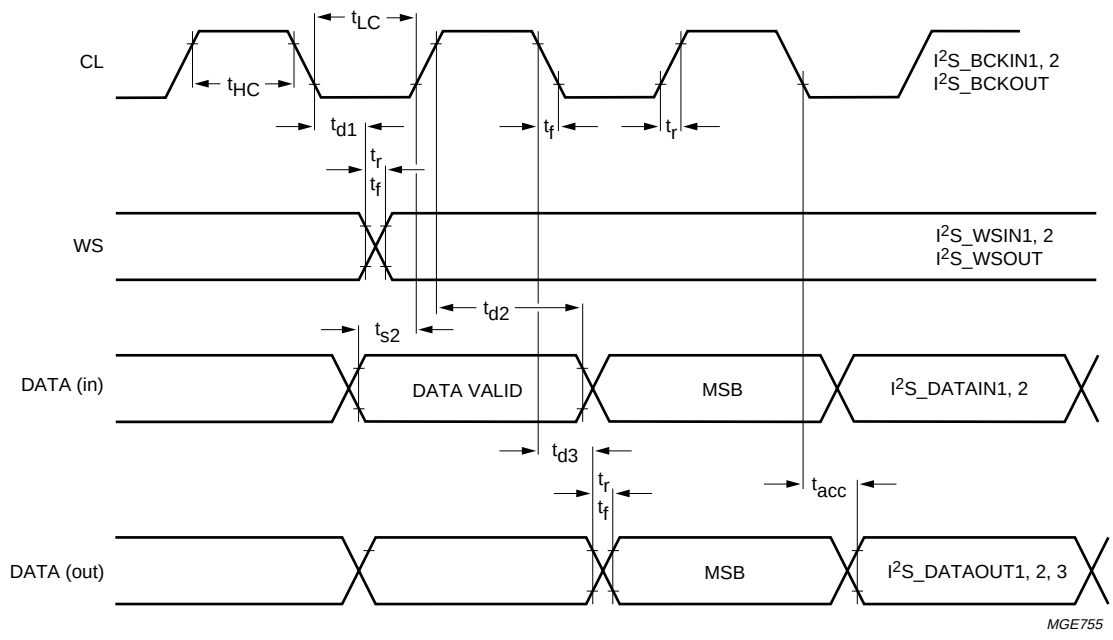


Fig.6 Timing diagram of I²S-bus output interface.

I²C-bus control and commands

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to the V_{DDX} via a pull-up resistor when connected to the output stages of a microprocessor. Data transfer can only be initiated when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals. The maximum clock frequency is 100 kHz (see Fig.7).

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Fig.8).

DATA TRANSFER

A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Fig.9).

ACKNOWLEDGE

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition (see Fig.10).

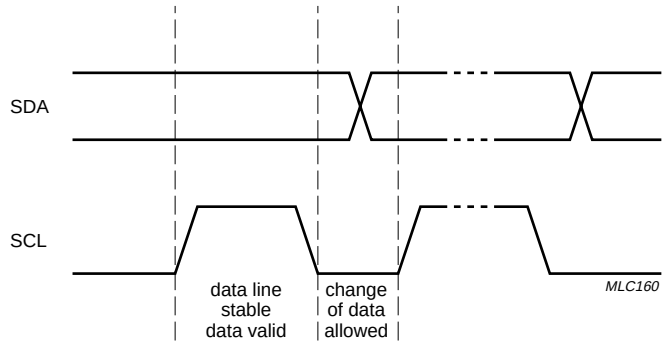


Fig.7 Bit transfer on the I²C-bus.

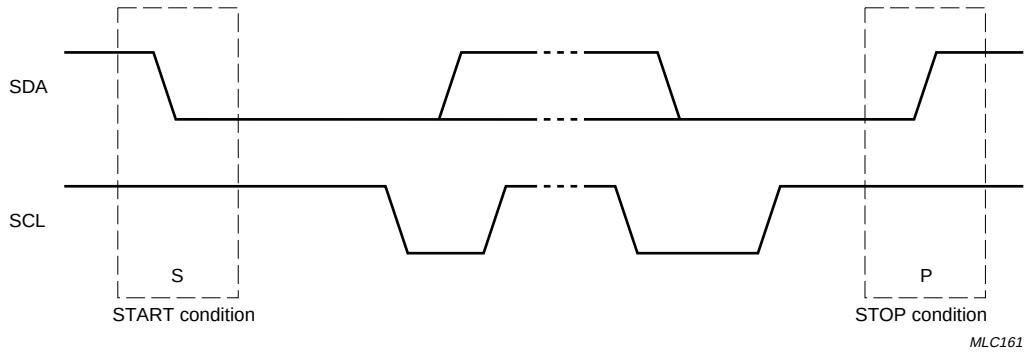


Fig.8 START and STOP conditions.

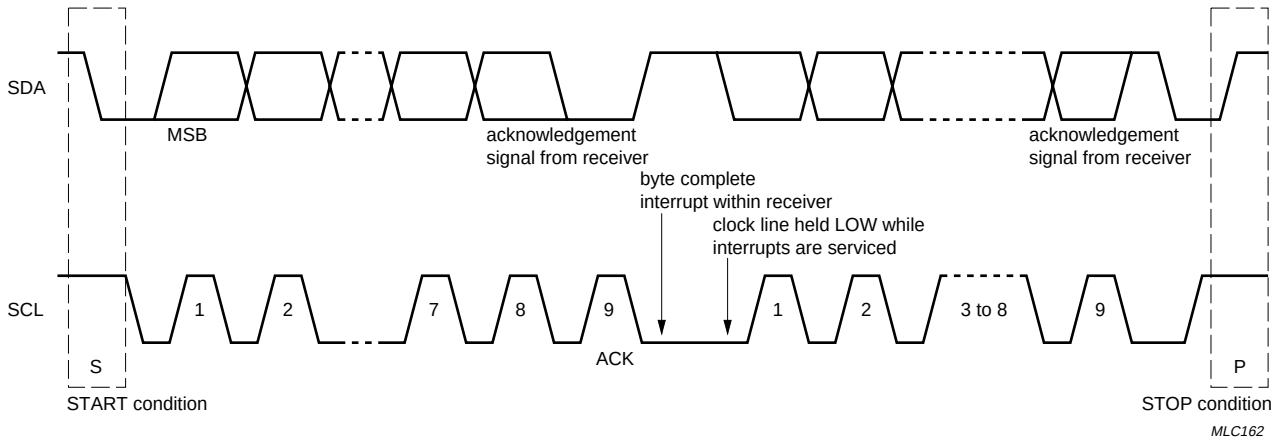


Fig.9 Data transfer on the I^2C-bus.

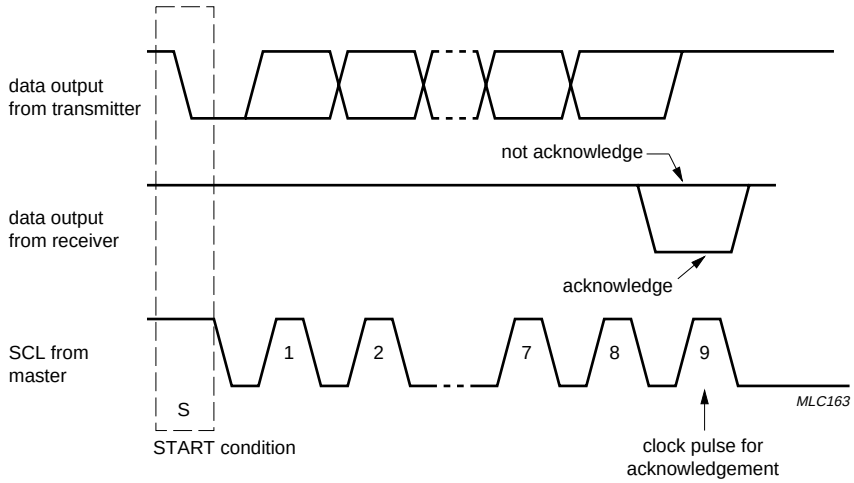


Fig.10 Acknowledge on the I²C-bus.

I²C-BUS FORMAT

Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the START procedure.

Slave address (pin A0)

The chip acts as a slave receiver or a slave transmitter. Therefore the clock signal SCL is only an input signal. The data signal SDA is a bidirectional line. The chip slave address is shown in Table 2.

The sub address bit A0 corresponds to the hardware address pin A0 which allows the device to have 1 of 2 different addresses.

Write cycles

The I²C-bus configuration for a write cycle is shown in Fig 12. The write cycle is used to write in the input selector control register and to initialise or update coefficient values.

The data length is 2 bytes or 3 bytes depending of the accessed memory. If the Y-memory is addressed the data length is 2 bytes, in case of the X-memory the length is 3 bytes. The slave receiver detects the address and adjusts the bytes accordingly.

Read cycles

The I²C-bus configuration for a Read cycle is shown in Fig 13. The read cycle is used to read data values from XRAM or YRAM.

I²C-BUS FUNCTION BITS

Input selector control register

The write only, two byte, input selector control register is located on absolute address 0FFFH (4095) and consists of 16 bits, starting with bit 0 and ending with bit 15.

Deviation from the I²C-bus specification

1. The data hold time ($t_{HD;DAT}$) for this device (≥0 ns as stated in the I²C-bus specification) should be as follows:
   a) For the crystal oscillator mode ($\overline{SHTCB}$ = 0):
   $$\geq\left(\frac{6}{f_{xtal}}\right)$$
   b) For the slave oscillator mode ($\overline{SHTCB}$ = 0):
   $$\geq\left(\frac{6}{f_{slave}}\right)$$
   c) For the slave oscillator mode ($\overline{SHTCB}$ = 1):
   $$\geq\left(\frac{3}{f_{slave}}\right)$$

During the write cycle, the I²C-bus clock frequency must be reduced.

The I²C-bus clock frequency has the following constraints:

$f_s > 2 \times f_{IIC}$

f_s = I²S-bus sampling frequency

f_{IIC} = I²C-bus clock frequency

If this constraint cannot be met, a higher I²C-bus frequency can be obtained in one of two ways:

1. By making the I²C-bus master insert a delay (t_d) after the acknowledge pulse (see Fig.11). The delay should be larger than or equal to $1/f_s$ where f_s is the I²S-bus sampling frequency.
2. By not using the auto-increment feature. This means that each data word must be preceded by its intended destination address.

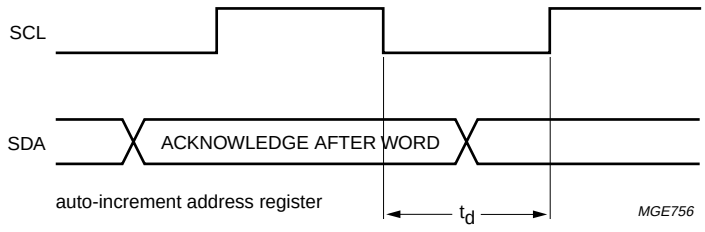


Fig.11 Timing of reduced I²C-bus frequency.

Table 2 Slave address

MSB							LSB
0	0	1	1	1	1	A0	R/$\overline{W}$

Table 3 Location of input selector control register bits in I²C-bus serial transmission; note 1

MSB																	LSB	
DATAH									DATAL									
15	14	13	12	11	10	9	8	A	7	6	5	4	3	2	1	0	A	P

Note

1. Explanation for the contents of the register bits:
   a) A = standard I²C-bus acknowledge.
   b) Number = bit number according to Table 4.
   c) P = standard I²C-bus STOP condition.

Table 4 Input selector control bits

SYMBOL	FUNCTION	NUMBER OF BITS	ON RESET	BIT NO
SEL-IN1/IN2	I²S input 1 or I²S input 2 input	1	IN1(0)	5
DIS_BCKWS	disable I²S_BCKOUT and I²S_WSOUT	1	enable(0)	7
ENA-I²S3	enable I²S_DATAOUT3	1	disable(0)	13
IMODE	I flag resets/background tasking	1	resets(0)	15

XRAM format

The XRAM block consists of 256 18-bit RAM locations 0 to 255 and is located on the absolute address range of 0000H to 00FFH. The I²C-bus transfer consists of 18 useful bits out of 24 bits.

Table 5 Format XRAM bits; note 1

MSB																								LSB	
DATAH									DATAM									DATAL									
D	D	D	D	D	D	17	16	A	15	14	13	12	11	10	9	8	A	7	6	5	4	3	2	1	0	A	P

Note

1. Explanation for the contents of the register bits:
   a) D = contents of I²C-bus data register bit is don't care.
   b) A = standard I²C-bus acknowledge.
   c) Number = bit number being useful bit XRAM memory.
   d) P = standard I²C-bus STOP condition.

YRAM format

The YRAM block consists of 256 12-bit RAM locations 0 to 255 and is located on the absolute address range of 0800H to 08FFH. The I^2C-bus transfer consists of 12 useful bits out of 16 bits.

Table 6 Format YRAM bits; note 1

MSB																	**LSB**	
DATAH									**DATAM**									
D	D	D	D	11	10	9	8	A	7	6	5	4	3	2	1	0	A	P

Note

1. Explanation for the contents of the register bits:
   a) D = contents of I^2C-bus data register bit is don't care.
   b) A = standard I^2C-bus acknowledge.
   c) Number = bit number being useful bit XRAM memory.
   d) P = standard I^2C-bus STOP condition.

Error processing

If a read action is done without first initialising the memory address the acknowledge after the read command will not be generated by the chip. This should be treated as an error message:

Table 7

S Write ACK ADDRH ACK ADDRL ACK S Read	Correct read sequence
S Read NEG ACK	Incorrect read sequence; address is not initialized

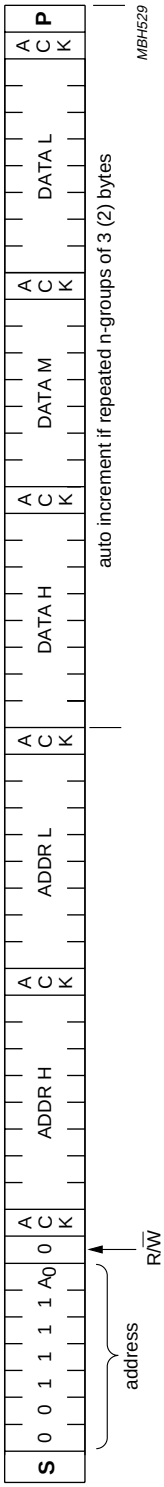


Fig.12 Master transmitter writes to chip.

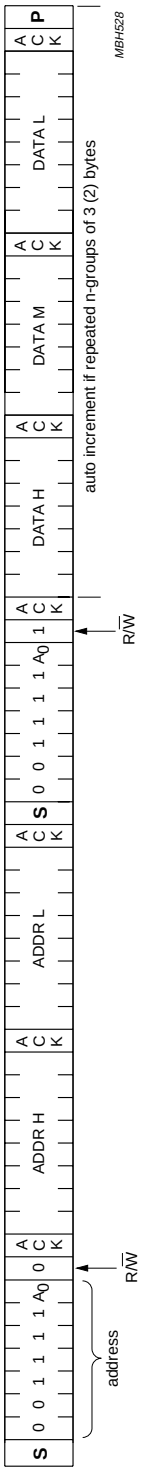


Fig.13 Master transmitter reads from chip.

$\overline{\text{DSP\_RESET}}$

The $\overline{\text{DSP\_RESET}}$ pin is active LOW and has an internal pull-up resistor. To enable a proper switch-on of the supply voltage a capacitor should be connected between this pin and V_{SS}. The capacitor value is such that the chip is in a reset state as long as the power supply is not stabilized.

The $\overline{\text{DSP\_RESET}}$ has the following functions:

- The bits of the input selector control register are set to logic 0 (see Table 4)
- The program counter is set to address 0000H
- The I^2C-bus interface is initialised; the SDA pin is guaranteed high-impedance.

When the level on the $\overline{\text{DSP\_RESET}}$ pin is HIGH, the DSP program starts to run.

When the level on the $\overline{\text{DSP\_RESET}}$ pin is low, the SDA pin is asynchronously set to a high-impedance state. In the absence of a clock and during the power-up reset, the SDA line is high-impedance.

TEST MODE CONNECTIONS (TSCAN, $\overline{\text{RTCB}}$ AND $\overline{\text{SHTCB}}$ PINS)

The TSCAN, $\overline{\text{RTCB}}$ and $\overline{\text{SHTCB}}$ pins are used to put the chip in test mode and to test the internal connections. Each pin has an internal pull-down resistor to ground. In the application these pins can be left open-circuit or connected to ground.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	DC supply voltage		–0.5	+6.5	V
ΔV_{DD}	voltage difference between two V_{DDx} pins		–	550	mV
$V_{i(max)}$	maximum input voltage		–0.5	V_{DD} + 0.5	V
I_{IK}	DC input clamp diode current	V_i < –0.5 V or V_i > V_{DD} + 0.5 V	–	10	mA
I_{OK}	DC output clamp diode current output type 4 mA	V_o < –0.5 V or V_o > V_{DD} + 0.5 V	–	20	mA
I_O	DC output source or sink current output type 4 mA	–0.5 V < V_o < V_{DD} + 0.5 V	–	20	mA
I_{DD}	DC output source or sink current output type 4 mA	–0.5 V < V_o < V_{DD} + 0.5 V	–	20	mA
I_{DD}	DC V_{DD} supply current per pin		–	50	mA
I_{SS}	DC V_{SS} supply current per pin		–	50	mA
V_{ESD}	ESD sensitivity for all pins				
	human body model	100 pF; 1500 Ω	3000	–	V
	machine model all pins except pin OSC	200 pF; 2.5 μH; 0 Ω	300	–	V
	machine model pin OSC	200 pF; 2.5 μH; 0 Ω	250	–	V
LTCH	latch-up protection	CIC spec/test method	100	–	mA
P_{tot}	total power dissipation		–	700	mW
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	57	K/W

DC CHARACTERISTICS

$V_{DD1} = V_{DD2} = V_{DD3} = V_{DD\_XTAL}$ = 4.5 to 5.5 V; T_{amb} = –40 to +85 °C; note 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDtot}	total DC supply voltage		4.5	5	5.5	V
$I_{DD(tot)}$	total DC supply current	DSP frequency = 18 MHz; maximum activity DSP	–	50	55	mA
P_{tot}	total power dissipation	DSP frequency = 18 MHz; maximum activity DSP	–	250	300	mW
V_{IH}	HIGH level input voltage all digital inputs and I/Os	pin types I1, I2 and I3	$0.7V_{DDX}$	–	–	V
		pin type I4	$0.8V_{DDX}$	–	–	V
V_{IL}	LOW level input voltage all digital inputs and I/Os	pin types I1, I2 and I3	–	–	$0.3V_{DDX}$	V
		pin type I4	–	–	$0.2V_{DDX}$	V
V_{hys}	hysteresis voltage	pin type I4	–	$0.33V_{DDX}$	–	V
V_{OH}	HIGH level output voltage digital outputs	V_{DDX} = 4.5 V; I_o = –4 mA; pin type O1 and O2	4.0	–	–	V
V_{OL}	LOW level output voltage digital outputs	V_{DDX} = 4.5 V; I_o = 4 mA; pin types I3, O1 and O2	–	–	0.5	V
$\lvert I_{LI} \rvert$	input leakage current	V_i = 0 or V_{DDX} voltage; pin type I1	–	–	1	µA
$\lvert I_{LO} \rvert$	output leakage current 3-state outputs	V_o = 0 or V_{DDX} voltage; pin type I3 and O2	–	–	5	µA
$R_{pu(VDDX)(int)}$	internal pull-up resistor to V_{DDX}	pin type I4	17	–	134	kΩ
$R_{pd(VSSD)(int)}$	internal pull-down resistor to V_{SSD}	pin type I2	17	–	134	kΩ
Crystal oscillator						
V_{DDX}	positive supply voltage crystal oscillator		4.5	5	5.5	V

Note

1. $V_{DDX} = V_{DD\_XTAL}$.

AC CHARACTERISTICS

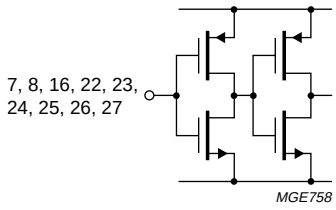
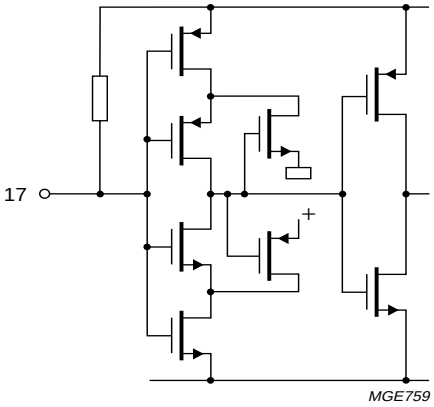
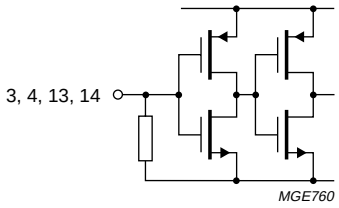
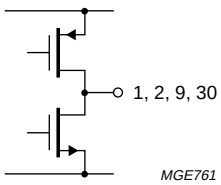
$V_{DD1} = V_{DD2} = V_{DD3} = V_{DD\_XTAL}$ = 4.5 to 5.5 V; T_{amb} = 25 °C; unless otherwise specified.

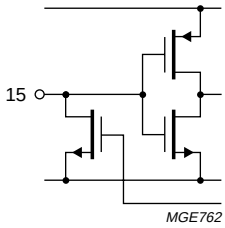
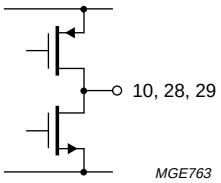
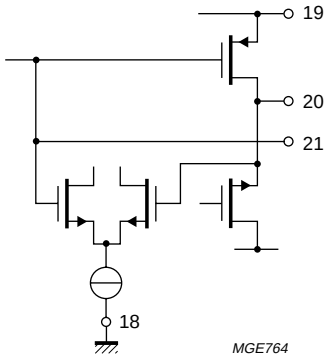
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{xtal}	crystal frequency	see Fig.3	–	–	36.864	MHz
α_f	spurious frequency attenuation		20	–	–	dB
I_{xtal}	current through crystal	at input voltage swing 0.2 V	–	500	–	μA
$g_{m(XTAL)}$	transconductance	at start-up	4	8	–	mS
V_{xtal}	voltage across crystal	note 1	–	500	–	mV
$C_{L(XTAL)}$	load capacitance		–	25	–	pF
R_{xtal}	allowed loss resistor of crystal	C_p = 5 pF; C1 = 10 pF; C2 = 10 pF	–	20	60	Ω
Slave oscillator						
f_{slave}	slave frequency	no divider; see Fig.4	–	–	18.432	MHz
SLVOLT	slave drive voltage	see Fig.4	3.75	–	–	V
t_r	input rise times	0.1 to 0.9V_{DD_XTAL}; note 2	–	–	20	ns
t_f	input fall times	0.1 to 0.9V_{DD_XTAL}; note 2	–	–	20	ns
Timing						
I²C-BUS INPUTS/OUTPUT						
t_f	fall time I²C-bus	0.1 to 0.9V_{DD}	–	5.7	–	ns
$f_{i(max)}$	maximum input frequency	SDA, SCL	–	–	100	kHz
I²S-BUS INPUTS/OUTPUTS						
t_r	rise time I²S-bus (O2)	C_L = 30 pF; 0.1 to 0.9V_{DD}	–	7.3	–	ns
t_f	fall time I²S-bus (O2)	C_L = 30 pF; 0.1 to 0.9V_{DD}	–	8.3	–	ns
t_{HC}	CL pulse width HIGH		112	–	–	ns
t_{LC}	CL pulse width LOW		112	–	–	ns
t_{d1}	WS out delay time		0	–	–	ns
t_{d2}	data in hold time		0	–	–	ns
t_{s2}	data in set-up time		25	–	–	ns
t_{d3}	data out delay time		0	–	5	ns
t_{acc}	data out access time		–	–	5 + 0.5 × C_L[3]	ns
ALL OTHER OUTPUTS (O1)						
t_r	rise time	C_L = 30 pF; 0.1 to 0.9V_{DD}	–	7.3	–	ns
t_f	fall time	C_L = 30 pF; 0.1 to 0.9V_{DD}	–	8.3	–	ns
ALL OTHER INPUTS						
t_r	input rise times	V_{DD} = 5.5 V	–	6	200	ns
t_f	input fall times	V_{DD} = 5.5 V	–	6	200	ns

Notes

1. The load capacitance is the sum of the series connection of C1 and C2 (see Fig.3) and the parasitic parallel capacitor of the crystal C_p.
2. With a 50%, ±5% duty cycle on oscillator drive input (see Fig.4).
3. The value for the capitative load C_L is given in pF.

INTERNAL CIRCUITRY

PIN NO.	PIN NAME	PIN TYPE	DC VOLTAGE (V)	INTERNAL CIRCUIT
7	DSP_IN1	I1		
8	DSP_IN2	I1		
16	SCL	I1		
22	I^2S_BCKIN1	I1		
23	I^2S_WSIN1	I1		
24	I^2S_DATAIN1	I1		
25	I^2S_DATAIN2	I1		
26	I^2S_WSIN2	I1		
27	I^2S_BCKIN2	I1		
17	$\overline{\text{DSP\_RESET}}$	I4		
3	$\overline{\text{RTCB}}$	I2		
4	$\overline{\text{SHTCB}}$	I2		
13	TSCAN	I2		
14	A0	I1		
1	I^2S_WSOUT	O2		
2	I^2S_BCKOUT	O2		
9	DSP_OUT1	O2		
30	I^2S_DATAOUT3	O2		

PIN NO.	PIN NAME	PIN TYPE	DC VOLTAGE (V)	INTERNAL CIRCUIT
15	SDA	I3		
10	DSP_OUT2	O1		
28	I^2S_DATAOUT1	O1		
29	I^2S_DATAOUT2	O1		
5	V_{DD1}		tbf	
6	V_{SS1}		0	
11	V_{SS2}		0	
12	V_{DD2}		5	
31	V_{SS3}		0	
32	V_{DD3}		5	
21	OSC		tbf	
20	XTAL		tbf	
19	V_{DD_XTAL}		5	
18	V_{SS_XTAL}		0	

APPLICATION INFORMATION

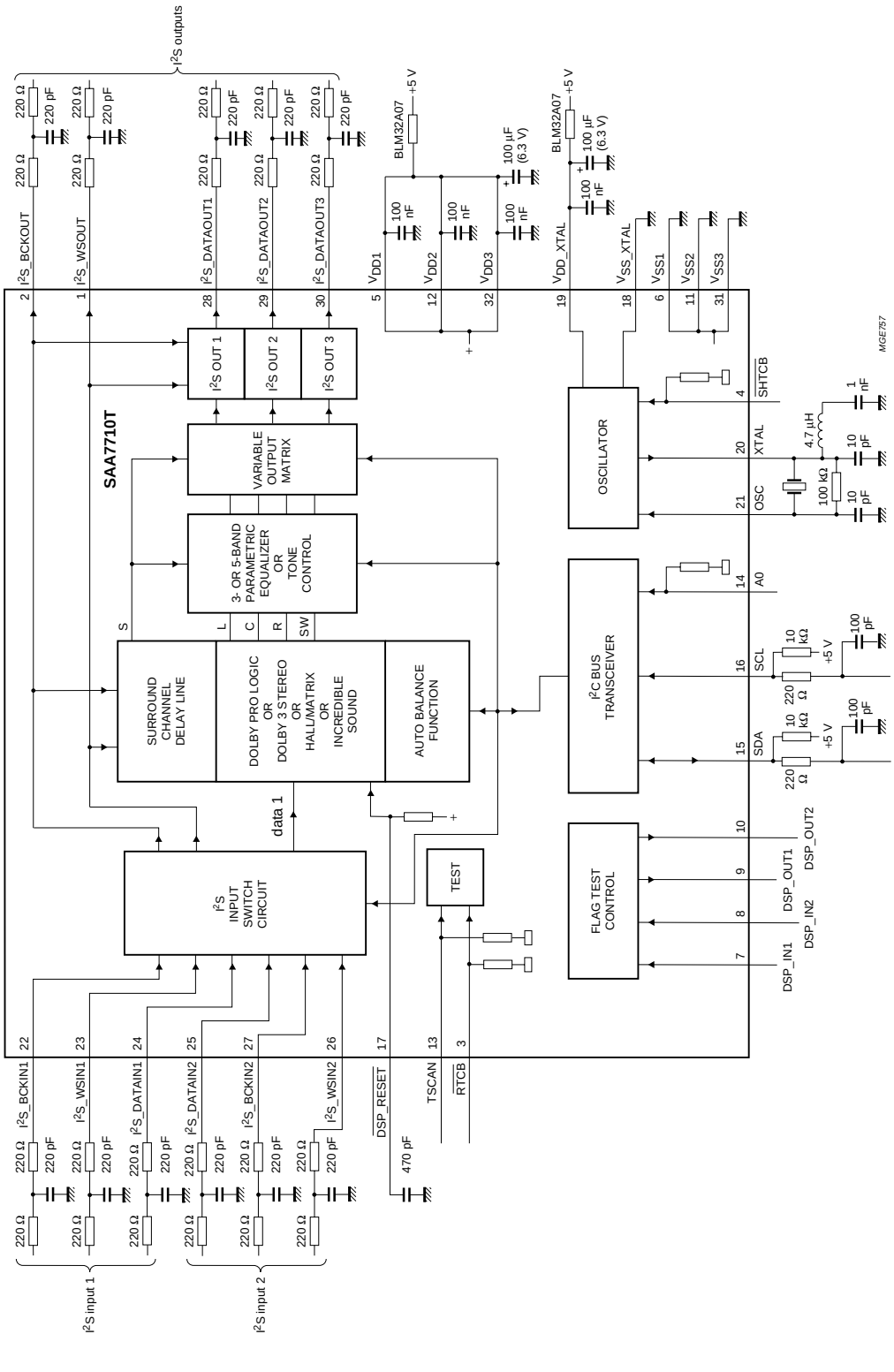
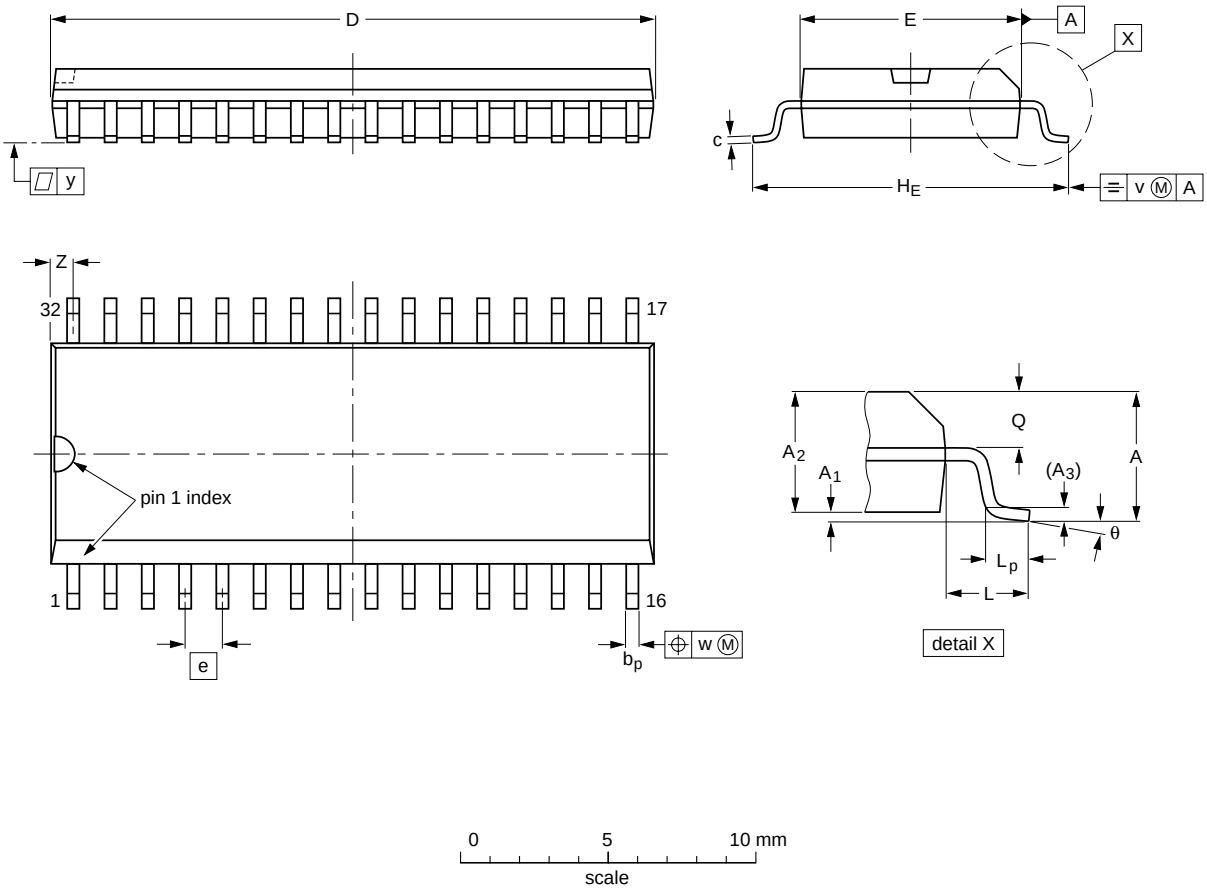


Fig.14 Application diagram.

PACKAGE OUTLINE

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.086	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT287-1						~~95-01-25~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Data sheet status	
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Product specification	This data sheet contains final product specifications.
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Printed in The Netherlands 547027/1200/02/pp28 Date of release: 1997 Aug 01 Document order number: 9397 750 02263

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